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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/761,204	01/22/2004	Noriaki Oda	8017-1122	2345

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EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 10/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/761,204	ODA, NORIAKI	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,14 and 42-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,14 and 42-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Serial Number: 10/761204 Attorney's Docket #: 8017-1122
Filing Date: 1/22/2004; claimed foreign priority to 1/30/2003

Applicant: Oda Examiner: Alexander Williams

Applicant's Amendment filed 7/24/06 to the election of the species of figure 2 (claims 1 to 11, 14 and 42 to 49), filed 8/30/05, has been acknowledged.

Claims 2, 12, 13 and 15 to 41 have been cancelled.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3 to 11, 14 and 42 to 49 are rejected under 35 U.S.C. § 102(e) as being anticipated by Suzuki et al. (U.S. Patent # 6,780,757 B2).

1. Suzuki et al. (figures 1 to 17) specifically figures 16 and 17 show a semiconductor device, comprising: a bonding pad **37**

on a semiconductor substrate **1,2;** an upper copper layer **26** on a lower surface of said bonding pads with a barrier metal interposed; and a lower copper layer **(left side 16)** closer to said semiconductor substrate than said upper copper layer; wherein a copper area ratio of said lower copper layer under said bonding pad is lower than that of said upper copper layer, and wherein said lower copper layer is not electrically connected to said upper copper layer under said bonding pad.

(32) As shown in FIG. 16, an upper film is further deposited on the aluminium alloy (Al--Si--Cu) film 33. The upper film is constituted of a single-layered titanium nitride (TiN) film 34 (60 nm in film thickness). In other words, any titanium (Ti) film is not formed on the aluminium alloy (Al--Si--Cu) film 33. If a titanium (Ti) film is provided, the compound of titanium and the aluminium alloy is formed, thereby causing the bonding failure. As a mater of course, if a titanium (Ti) film is not provided, the compound of aluminium and the nitride is formed on the surface of the aluminium alloy film. However, this compound can be removed during the step of removing the titanium nitride at the time of making an opening for the bonding pad. After the deposition of the aluminium alloy (Al--Si--Cu) film 33, the re-flowing as set out hereinbefore may be carried out to cause the surface to be more flattened. Alternatively, after the deposition of the aluminium alloy (Al--Si--Cu) film 33, the semiconductor substrate may be removed to outside of the sputtering apparatus, and thus the aluminium alloy (Al--Si--Cu) film 33 may be exposed to the air to form an oxide film on the surface thereof.

(35) Next, as shown in FIG. 17, part of the passivation film 36 is made with a hole by dry etching using photoresist as a mask, thereby exposing part of the aluminium (Al) interconnection film 35 to form a bonding pad 37. The upper film on the surface of the bonding pad 37 (Al interconnection 35) is constituted of the single-layered titanium nitride (TiN) film 34 (provided that where the Al--Si--Cu film 33 is oxidized on the surface thereof, it is made of TiN film and oxide film). Accordingly, the bonding pad 37 is not deposited with the compound of aluminium (Al) and titanium (Ti) unlike the case where the upper film is constituted of a builtup film of the titanium nitride (TiN) film and the titanium (Ti) film.

3. A semiconductor device according to claim 1, Suzuki et al. show wherein the copper area ratio of said upper copper layer is greater than that of other copper layers that are formed as circuit interconnects on said semiconductor substrate.

4. A semiconductor device according to claim 1, Suzuki et al. show wherein the copper area ratio of said upper copper layer is at least 70%.

5. A semiconductor device according to claim 1, Suzuki et al. show wherein the planar dimensions of said bonding pads and said upper copper layer are substantially equal.

6. A semiconductor device according to claim 1, Suzuki et al. show wherein said upper copper layer is constituted by a plurality of copper layers.

7. A semiconductor device according to claim 6, Suzuki et al. show wherein the copper area ratios of each copper layer of said upper copper layer are substantially the same.

8. A semiconductor device according to claim 6, Suzuki et al. further comprising: interlevel dielectric films that are provided between each of the copper layers of said upper copper layer; and via-plugs composed of copper that are embedded in said interlevel dielectric films wherein each of the copper layers of said upper copper layer are connected by way of said via-plugs.

9. A semiconductor device according to claim 8, Suzuki et al. show wherein the copper layer pattern of the copper layer

that is positioned uppermost in said upper copper layer and said via-plugs that are connected to the copper layer pattern are embedded in a dielectric film that is composed of a first material.

10. A semiconductor device according to claim 1, Suzuki et al. show wherein the copper area ratio of said lower copper layer is at least 15% and not greater than 95%.

11. A semiconductor device according to claim 1, Suzuki et al. show wherein said lower copper layer is constituted by a plurality of copper layers.

14. A semiconductor device according to claim 13, Suzuki et al. show wherein each of the copper layers of said lower copper layer are constituted by a copper pattern that is embedded in a dielectric film that is composed of a second material having a lower relative dielectric constant than said first material.

Initially, it is noted that the 35 U.S.C. § 103 rejection based on a plurality of copper layers and a copper layer deals with an issue (i.e., the integration of multiple pieces into one piece or conversely, using multiple pieces in replacing a single piece) that has been previously decided by the courts.

In Howard v. Detroit Stove Works 150 U.S. 164 (1893), the Court held, "it involves no invention to cast in one piece an article which has formerly been cast in two pieces and put together...."

In In re Larson 144 USPQ 347 (CCPA 1965), the term "integral" did not define over a multi-piece structure secured as a single unit. More importantly, the court went further and stated, "we are inclined to agree with the solicitor that the

use of a one-piece construction instead of the [multi-piece] structure disclosed in Tuttle et al. would be merely a matter of obvious engineering choice" (bracketed material added). The court cited In re Fridolph for support.

In re Fridolph 135 USPQ 319 (CCPA 1962) deals with submitted affidavits relating to this issue. The underlying issue in In re Fridolph was related to the end result of making a multi-piece structure into a one-piece structure. Generally, favorable patentable weight was accorded if the one-piece structure yielded results not expected from the modification of the two-piece structure into a single piece structure.

Claims 42-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. (U.S. Patent # 6,780,757 B2).

42. Suzuki et al. (figures 1 to 17) specifically figures 16 and 17 show a semiconductor device comprising: a bonding region in which a bonding pad **37** is formed; an internal circuit region provided inside of said bonding region, said internal circuit region having a multilevel wiring structure that includes a plurality of copper interconnect layers at **35** a first level and a plurality of copper interconnect layers **26** at second level; and

a copper layer **16** formed in said bonding region under said bonding pad in electrical contact therewith, one of said copper interconnect layers at said first level being elongated from said internal circuit region to said bonding region under said copper layer in electrical isolation therefrom.

43. The device as claimed in claim 42, Suzuki et al. show wherein one of said copper interconnect layers at said second level is further elongated from said internal circuit region to said bonding region under said copper layer in electrical

isolation from said copper layer and from one of said copper interconnect layers at said first level.

44. The device as claimed in claim 42, Suzuki et al. show wherein said copper layer includes first and second copper layers and a via-plug sandwiched therebetween.

45. The device as claimed in claim 44, Suzuki et al. show wherein said multilevel wiring structure further includes a plurality of copper interconnect layers at a third level and a plurality of copper interconnect layers at a fourth level, said first copper layer being formed at said third level and said second copper layer being formed at said fourth level.

46. The device as claimed in claim 45, Suzuki et al. show wherein said bonding pad is in electrical contact with said second copper layer, and one of said copper interconnect layers at said fourth level has an electrical contact with said second copper layer.

Therefore, it would have been obvious to one of ordinary skill in the art to use the copper layer and the plurality of copper layers as "merely a matter of obvious engineering choice" as set forth in the above case law.

Response

Applicant's arguments filed 7/24/06 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

The listed references are cited as of interest to this application, but not applied at time.

Field of Search	Date
U.S. Class and subclass: 257/700,701,758,459,784,774,680,756,750,734,751,760,762,E23.02,E23.145,E21.582,E21.576	9/30/05 4/5/06 10/11/06
Other Documentation: foreign patents and literature in 257//700,701,758,459,784,774,680,756,750,734,751,760,762,E23.02,E23.145,E21.582,E21.576	9/30/05 4/5/06 10/11/06
Electronic data base(s): U.S. Patents EAST	9/30/05 4/5/06 10/11/06

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
10/11/06